NJU6676
Application Note

New Japan Radio Co.,Ltd.

Frame Frequency

-Using the Built-in Oscillator(CLS="H")

fFR (Frame Frequency) = fOSC/(4x65)
fCL(display clock) =fOSC/4

Ex. fOSC = 22KHz
fFR = 84.6 Hz
fCL(output) = 5.5KHz

-Using a External Oscillator and the Built-in Voltage Booster (CLS="H", external clock signal inputted into OSC1 pin)

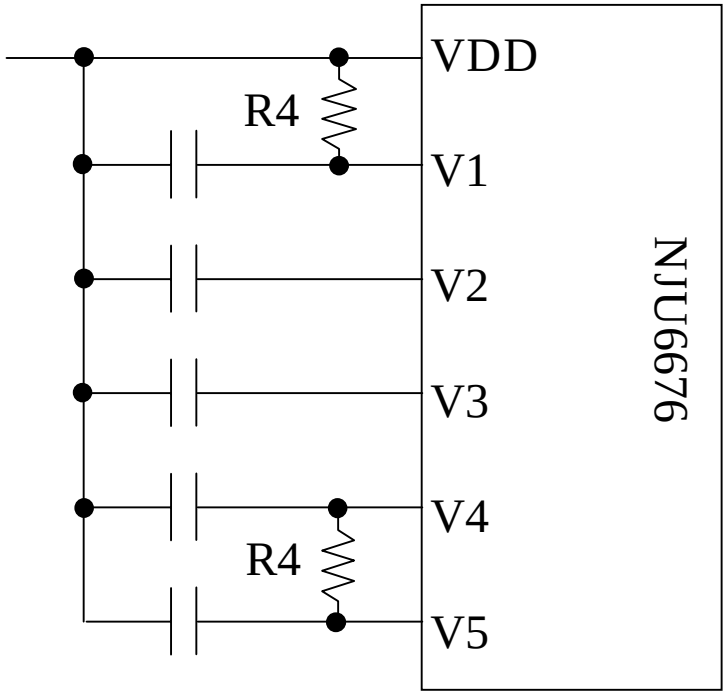
fFR = OSC1/(4x65)
fCL(output) = fOSC/4

-Using External Oscillator and Power Supply (CLS="L", external clock signal inputted into CL pin)

fFR =fCL/65
fCL(input) =CL

LCD Bias Voltage Generator

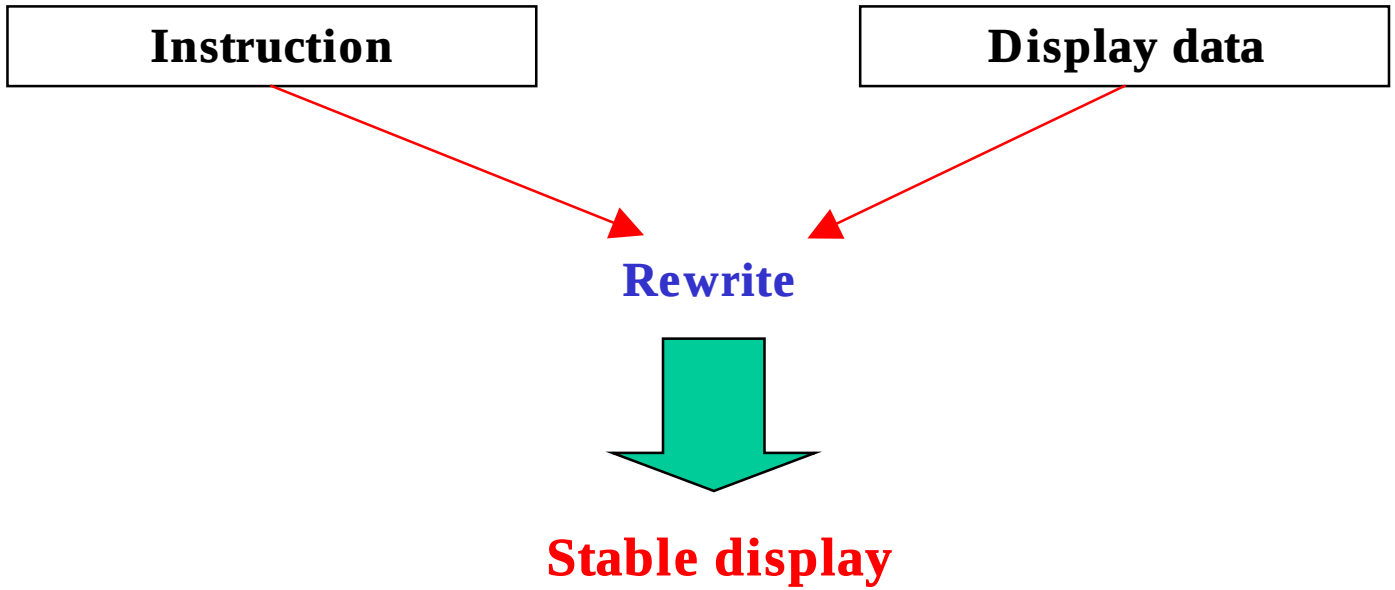
When the built-in power supply circuit is used, for big panel, because the alternating and direct current consumption is bigger than the small one's, the bias voltage V1 and V4 is susceptible to change. To stabilize V1 and V4, the external resistors connecting like below is recommended. About resistor's value , please confirm with your practical application.



For reference: R4 = 68KΩ ~
(by our testing R4 is from 68KΩ to 150KΩ)

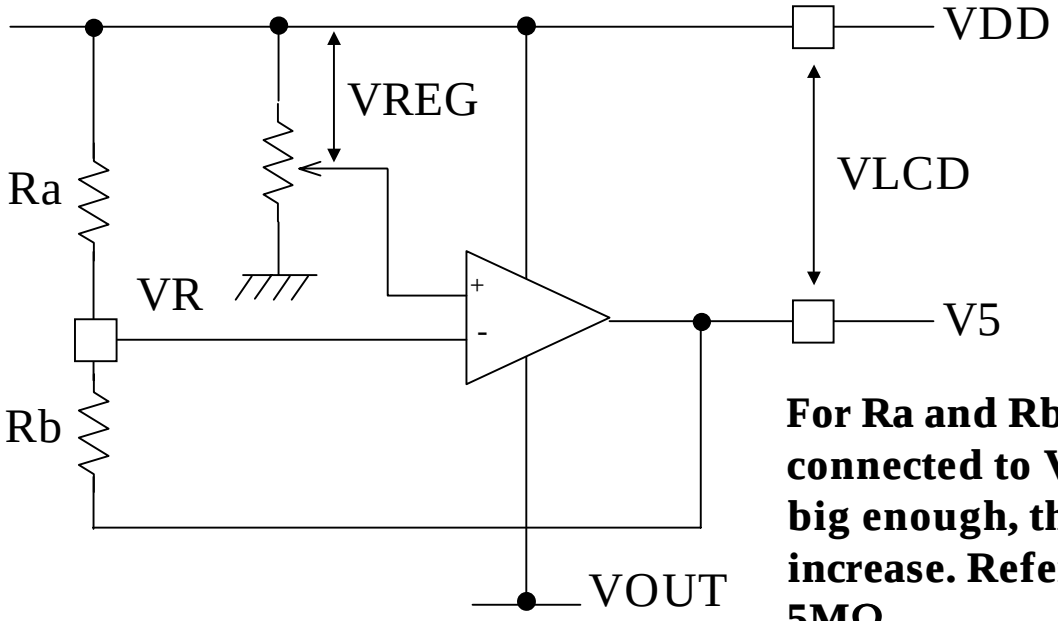
Refresh Display

To stabilize the display, please refresh the instruction and display data at a constant frequency.
Further more, if the reset instruction data is the same as before, there is no effect on display.



Voltage Regulator

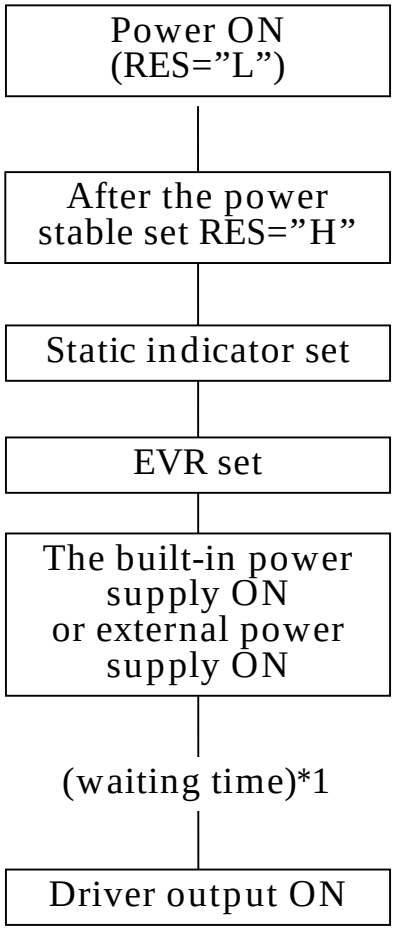
The built-in Voltage Booster generates Vout, then Vout is regulated by the Voltage Regulator and outputted as V5.
The LCD driving voltage VLCD (= VDD-V5) can be adjusted by external Ra and Rb. No matter how the built-in voltage booster is set, it is impossible to obtain VLCD higher than Vout.



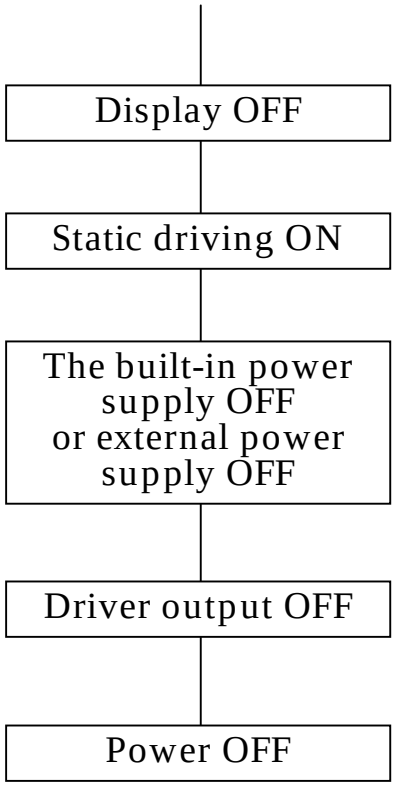
For Ra and Rb, because they are directly connected to VDD-V5, if the resistance is not big enough, the current consumption will increase. Reference value: Ra + Rb = 1MΩ ~ 5MΩ.

Sequence of Power ON/OFF(1)

- Power ON



- Power OFF



*1: The waiting time for the built-in power supply stabilizing will vary with the C_{OUT}, C_1~C_8, V_{DD}, and V_{LCD}. Please confirm with practical application.

Sequence of Power ON/OFF(2)

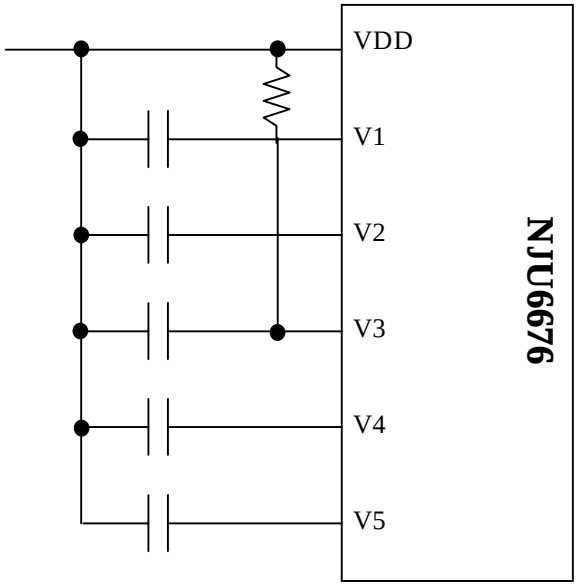
If electrons are left in the stabilizing capacitor, which are connected to V1~V5 pins, when the power ON/OFF, unexpected pixels maybe turned on for a time. This is because the discharge speed of the capacitors is different, result in the order change of the bias voltage V1~V5.

There for, if there is unexpected lighting pixels during power ON, set a waiting time before the driver outputting signal.

If there is unexpected lighting pixels during power OFF, insert a resistor between VDD and slowly discharging pin.

The resistance and waiting time will change a lot with different LCM, please confirm with practical application.

The figure shows that if V3 discharging speed is slow during power OFF, connect VDD and V3 with a 500KΩ ~ 5MΩ.



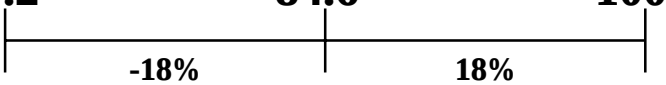
Specification of Oscillation Frequency

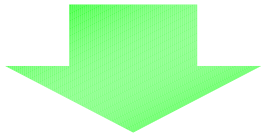
-Oscillation Frequency

	Min.	Typ.	Max.	
fOSC	18	22	26	[kHz]

-Frame Frequency = fOSC/(4x65)

	Min.	Typ.	Max.	
Frame Frequency	69.2	84.6	100	[Hz]





To avoid flicker phenomena, let frame frequency away from 50Hz~60Hz.